**Amendments to the Abstract**

Please replace the abstract with the following new abstract.

A latch circuit ~~(1)~~ comprising, a differential input with ~~an~~ a non-inverting input (D+) and an ~~a~~ [[non-]]inverting input (D-). The latch further comprises a differential output with ~~an~~ a non-inverting output (Q+) and an ~~a~~ [[non-]]inverting output (Q-). One of the outputs (Q-) is coupled to one of the inputs input (D+) having an opposite polarity. The latch further comprises a control input for receiving a control signal ($V_{cM}$) for determining a threshold for an input signal (In) such that if the input signal is at larger than the threshold the non-inverting output is in a HIGH logic state and in a LOW state if the input signal is smaller than the threshold~~, respectively~~.